Tran, Anh O.

From: David Snyder [dsnyder@antonelli.com]
Sent: Monday, August 15, 2005 5:25 PM
To: Tran, Anh O.
Subject: K. KANETANI et al - U.S.S.N. 10/754,596 - text for Examiner's Amendment
Importance: High

August 15, 2005

Dear Examiner Tran:

Thank you for your helpful comments during our telephone interview regarding the above matter.

In accordance with our discussion, enclosed please find a copy of amended claim 17 for the above-identified matter:

17. A semiconductor logic circuit according to claim 10, wherein:
said each reset circuit comprises:
a field effect transistor for preventing through state paths to the source and the drain of which are provided between said one terminal and said other terminal and the gate of which is controlled by said reset pulse;
a field effect transistor for reset paths to the source and the drain of which are provided between said first power source terminal and said other terminal and the gate of which is controlled by said reset pulse; and
a field effect transistor for precharge paths to the source and the drain of which are provided between said first power source terminal and said other terminal and the gate of which is controlled by said control signal.

If you have any questions regarding this claim, or would prefer to have it in some other form, please let me know.

Kindly acknowledge receipt of this email by return email.

Regards,

Gregory E. Montone